WHAT IS CLAIMED IS:

1. An integrated circuit, having an effective maximum delay of two gate delays from an input operably powered by a first power supply to first and second outputs operably powered by a second power supply, the first and second outputs having predetermined values during an interval when the first power supply has failed and the second power supply is active.

2. The integrated circuit, as recited in claim 1, wherein the first and the second power supplies are based at least in part on different power domains.

3. The integrated circuit, as recited in claim 1, wherein the first power supply is based at least in part on a core power domain and the second power supply is based at least in part on an I/O power domain.

4. The integrated circuit, as recited in claim 3, wherein the second power supply includes a voltage division of an I/O power supply.

5. The integrated circuit, as recited in claim 4, wherein the second power supply has a voltage level substantially equivalent to a voltage level of the first power supply.

6. The integrated circuit, as recited in claim 1, wherein the effective maximum delay from the input to each of the first and second outputs is substantially equivalent.

7. The integrated circuit, as recited in claim 1, wherein the first and second outputs have complementary values based on an input signal during an interval when the first power supply is active and the second power supply is active.

8. An integrated circuit comprising:
an input operably powered by a first power supply; and
a first and a second output operably powered by a second power supply,
wherein the integrated circuit has an effective maximum delay of two

gate delays from the input to the first and the second outputs, the first and second outputs having predetermined values during an interval when the first power supply has failed and the second power supply is active.

9. The integrated circuit, as recited in claim 8, further comprising:

a first and a second node coupled, respectively, to the first and the second outputs; and

a first and a second device coupled, respectively, to the first and the second nodes.

10. The integrated circuit, as recited in claim 9, wherein the first device is responsive to the first power supply and coupled to the second power supply.

11. The integrated circuit, as recited in claim 9, wherein the first device is configured as a diode.

12. The integrated circuit, as recited in claim 11, wherein the first device is a p-type transistor having a bulk coupled to the second power supply via an n-type device.

13. The integrated circuit, as recited in claim 8, wherein the first and the second power supplies are based on different power domains.

14. The integrated circuit, as recited in claim 13 wherein the first power supply is based at least in part on a core power supply.

15. The integrated circuit, as recited in claim 13, wherein the second power supply is based at least in part on an I/O power supply.

16. The integrated circuit, as recited in claim 15, wherein the second power supply is generated by voltage division of the I/O power supply.

17. The integrated circuit, as recited in claim 8, wherein the first and second outputs have complementary values based on the input during an interval when the first power supply is active and the second power supply is active.

18. The integrated circuit, as recited in claim 8, wherein the second power supply has a voltage level substantially equivalent to the voltage level of the first power supply.

19. The integrated circuit, as recited in claim 9, further comprising:

a first inverter coupled to the first node, the first output, and the second power supply; and

a second inverter coupled to the second node, the second output, and the second power supply.

20. The integrated circuit, as recited in claim 9, further comprising:

a transmission gate coupled to the input, the first node, the first power supply, and a third node.

21. The integrated circuit, as recited in claim 20, further comprising:

at least a third inverter coupled to the third node and the second power supply and responsive to the first power supply.

22. The integrated circuit, as recited in claim 8, embodied in computer readable descriptive form suitable for use in design, test, or fabrication of an integrated circuit.

23. A method comprising:

generating, based on an input operably powered by a first power supply, complementary signals for at least a first and a second output operably powered by a second power supply in at most two gate delays during an interval where the first power supply is active;

sensing a failure in the first power supply; and

respectively introducing predetermined signals to the first and second outputs during an interval when the first power supply has failed and the second power supply is active.

24. The method, as recited in claim 23, further comprising:
matching a first and second delay from the input to the first and the second outputs.

25. The method, as recited in claim 23, wherein the first and the second power supplies are based on different power domains.

26. The method, as recited in claim 23 wherein the first power supply is based at least in part on a core power supply of an integrated circuit.

27. The method, as recited in claim 23, wherein the second power supply is based at least in part on an I/O power supply.

28. The method, as recited in claim 23, further comprising:
substantially matching the voltage level of the second power supply to the voltage level of the first power supply.

29. The method, as recited in claim 27, wherein the second power supply is generated by voltage division of the I/O power supply.

30. An apparatus comprising:
means for generating complementary signals for at least a first and a second output from an input powered by a first power supply in at most two gate delays; and
means for introducing predetermined signals to the first and second outputs during an interval when the first power supply fails and a second power supply is active.

31. The apparatus, as recited in claim 30, further comprising:

means for matching a first and second delay from the input to the first and the second outputs.

32. The apparatus, as recited in claim 30, further comprising:

means for substantially matching a voltage level of the second power supply to a voltage level of the first power supply.